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10/526,990	03/07/2005	Shridhar Mubaraq Mishra	1890-0213	6999

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EXAMINER	
RUTKOWSKI, JEFFREY M	

ART UNIT	PAPER NUMBER
2473	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,990	MISHRA ET AL.	
	Examiner	Art Unit	
	JEFFREY M. RUTKOWSKI	2473	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-17 and 19-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-17 and 19-30* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim 1-7, 18 and 26-27 have been cancelled.

Examiner's Note

The status identifier for **claim 25** is incorrect. Since the word "MAC" was amended in the claim, it appears the status identifier should be "Currently Amended" and not "Previously Presented".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 8, 11, 16-17, 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte et al. (US Pat 7,099,276), hereinafter referred to as Kalkunte, in view of Moran et al. (US Pg Pub 2002/0071398), hereinafter referred to as Moran, and Takeuchi et al. (US Pat 5,233,603), hereinafter referred to as Takeuchi.

4. For **claims 8 and 17**, Kalkunte discloses *a plurality of Media Access Control (MAC) interfaces* (figure 20 shows a SOC has more than one MAC interface) *configured to receive/transmit Fast Ethernet (FE) packets* (20 ports are configured as bidirectional Fast Ethernet ports; see figure 20)*; at least one MAC interface configured to receive/transmit Gigabit Ethernet (GE) packets in a first mode of operation* (when the FE ports are trunked with the gigabit port, the FE ports are used to send and receive packets at gigabit speeds; see figure 20) *and to receive/transmit FE packets in a second mode of operation* (if the FE ports are not trunked with the GE port, then the FE ports send and receive packets at Fast Ethernet speeds; see figure 20)*; and wherein the ingress/egress port* (SOC; see figure 20) *operates as a single GE port in the first mode of operation using the at least one MAC interface to transmit and receive GE packets* (figure 20 shows that when trunking is used, there is a single GE port for ingress/egress communications; see figure 20) *and as more a plurality of FE ports in the second mode of operation using the plurality and the at least one MAC interface to transmit and receive FE packets* (when trunking is not used, the FE ports are released to be used as a plurality of FE ports; see figure 20).

5. Kalkunte discloses the use of flow control (see col. 36 lines 50-55), *transmit modules* (MAC_TX_FIFO **140**; see figure 10) and *input modules* (input FIFO **142**; see figure 14). Kalkunte does not disclose memory that interacts with all the MAC interfaces. Moran discloses *receive* (receive store **30** allocated in memory **14**; see paragraph 0032) *and transmit modules* (transmit store **29** allocated in memory **14**; see paragraph 0032) *which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces* (figure 1 shows a bus is used to send and receive information between

memory **14** and all the MAC interfaces **14**) *and wherein each MAC interface is associated with a separate buffer configured to store packets as they are received at the respective MAC interface* (see paragraph 0032). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Moran's arrangement in Kalkunte's invention to control the amount of bandwidth for a port (Moran, title).

6. The combination of Kalkunte and Moran discloses the use of a receive module. The combination does not disclose how packets are read from the memory **14** (see figure 1 of Moran). Takeuchi discloses *the receive module* (buffer units **2501-250N**; see figure 4) *being arranged to receive packets from the respective buffers sequentially* (the buffer units **2501-250N** sequentially receives packet from input buffers **1401** to **140N** sequentially; see col. 6 lines 9-11). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Takeuchi's arrangement in Kalkunte's invention to multiplex the received information (Takeuchi, col. 6 lines 9-11).

7. For **claim 11**, Kalkunte discloses *FE packets* are well-known in the art (see col. 1 lines 35-60). Kalkunte does not disclose the sequential reception of packets. Takeuchi suggests *the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously* (the packets are read from the input buffers **1401** to **140N** in a cyclical manner; see col. 6 lines 5-11). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Takeuchi's arrangement in Kalkunte's invention to multiplex the received information (Takeuchi, col. 6 lines 9-11).

8. For **claim 16**, Kalkunte discloses *wherein the plurality of MAC interfaces consists of 8 MAC interfaces* (see figure 20).

9. For **claim 19**, Kalkunte discloses *wherein the at least one ingress/egress port* (SOC; see figure 20) *comprises eight ingress/egress ports* (the SOC has 20 FE ports; see figure 20), *each ingress/egress port being configured to switch between a first mode* (link aggregated) *and a second mode* (not link aggregated), *in which each ingress/egress port operates as a single GE port* (figure 20 shows that when the FE ports are aggregated with one GE port, a single GE port is left for ingress/egress operations; see figure 20) *in the first mode and as eight FE ports in the second mode and wherein the switch can operate as n GE ports* (when the FE ports are not link aggregated each FE functions as a separate port; see figure 20) *and 8(8-n) FE ports for n a selectable integer in the range 0 and 8* (any number of device ports can be used; see col. 35 lines 35-45).

10. **Claims 9-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte in view of Moran and Takeuchi as applied to **claim 8** above, and further in view of Tzeng et al. (US Pg Pub 2003/0212815), hereinafter referred to as Tzeng.

11. For **claim 9**, the combination of Kalkunte, Moran and Takeuchi discloses *MAC interfaces* that can operate at both Fast Ethernet and Gigabit speeds (see paragraph 0003 of Moran). The combination of Kalkunte, Moran and Takeuchi does not disclose a particular arrangement for the MAC interfaces. Tzeng discloses *only one of the MAC interfaces is configured to receive/transmit both GE and FE packets* (GMAC/MAC **101**; see figure 1), *the other MAC interfaces only being adapted to receive/transmit FE packets* (MAC **106**; see figure 1). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Tzeng's arrangement in Kalkunte's invention to provide a switch that can be connected to many different types of network media (Tzeng, paragraph 0021).

12. For **claim 10**, Kalkunte of *FE packets* are well-known in the art (see col. 1 lines 35-60). Kalkunte does not disclose the sequential reception of packets. Takeuchi suggests *the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously* (the packets are read from the input buffers **1401** to **140N** in a cyclical manner; see col. 6 lines 5-11). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Takeuchi's arrangement in Kalkunte's invention to multiplex the received information (Takeuchi, col. 6 lines 9-11).

13. **Claims 12 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte in view of Moran and Takeuchi as applied to **claims 8, 17 and 14 respectively** above, and further in view of Gentry, Jr. (US Pat 6,356,951), hereinafter referred to as Gentry.

14. For **claims 12 and 20**, the combination of Kalkunte, Moran and Takeuchi, discloses *the receive module further includes a memory configured to store packet data* (Moran, paragraph 0032).

15. The combination of Kalkunte, Moran and Takeuchi do not teach the use of a receiver that interfaces with a parser. Gentry discloses an input port processing module **104** interfaces with a header parser **106 [figure 1A]**. The header parser **106** parses only the header (descriptor) portion of the packets **[col. 7 lines 50-55]** (a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a receiver interface in Kalkunte's invention to identify related packets **[Gentry, col. 7 line 53]**.

16. **Claims 13-15, 21-23 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte in view of Moran, Takeuchi and Gentry as applied to **claim 12 and 20** above, and further in view of Di Placido (US Pat 6,226,292).

17. For **claims 13, 15, 21, 23**, the combination of Kalkunte, Moran, Takeuchi and Gentry teach a receiver interface for fetching data the header parser **106** copies header information (descriptor) from input port processing module **104** into a header memory **302 [Gentry, col. 17 lines 8-9 and figure 3]** (claim 13: wherein the receiver interface is further configured to fetch packet data from the set of buffers and store the packet data in the memory; claim 15: wherein the receiver interface is further configured to store the descriptor associated with the packet data in the memory).

18. Kalkunte teaches the use of an input FIFO **142** input FIFO **142** (see figure 14). The combination of Kalkunte, Moran, Takeuchi and Gentry do not disclose the use of more than one receive buffers (set of buffers). Di Placido teaches a switch arrangement that contains more than one set of receive buffers **20 [figure 2]**. It would have been obvious to a person of ordinary skill in the art to use a set of buffers in Kalkunte's invention to manage memory space by a particular buffer to a particular MAC interface **[Di Placido, col. 4 lines 62-65]**.

19. For **claims 14 and 22**, Kalkunte discloses *wherein each buffer of the set of buffers comprises a FIFO buffer* (input FIFO **142**; see figure 14).

20. For **claim 30**, the combination of Kalkunte, Moran and Takeuchi do not teach the use of a receiver that interfaces with a parser. Gentry discloses *a parser* (header parser **106**) *for extracting information form headers in the received packets* (the header parser **106** parses the header portions of the packets; see col. 7 lines 50-65)*, and adding this information to the*

descriptor (this feature is suggested by Gentry because the header parser **106** can also extract other information from the packet, such as the packet length; see col. 8 lines 14-20). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Gentry's arrangement in Kalkunte's invention to identify related packets **[Gentry, col. 7 line 53]**.

21. **Claims 24-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte in view of Moran.

22. For **claim 24**, Kalkunte discloses *providing data packets to an ingress/egress port* (SOC; see figure 20) *of an Ethernet switch* (network switch; see col. 2 lines 49-61. Figure 1 shows the SOC **10** is integrated into a switch), *ingress/egress port having a plurality of Media Access Control (MAC) interfaces* (figure 20 shows the SOC has more than one MAC interface), *each MAC interface configured for receiving/transmitting Fast Ethernet (FE) packets* (there are interfaces for sending and receiving FE packets; see figure 20), *at least one of the MAC interfaces further being configured to receive/transmit Gigabit Ethernet (GE) packets independent of the other plurality of MAC interfaces* (figure 20 shows that some of the FE interfaces can be trunked and used to transmit and receive packets at gigabit speeds independently of the remainder of the FE ports) *and switching the ingress/egress port* (SOC; see figure 20) *between a first mode and a second mode, in which the ingress/egress port operates as a single GE port in the first mode* (when the FE ports are trunked with one of the GE ports, the SOC operates with only one GE port for ingress and egress communications) *and as more than one FE port in the second mode* (when the FE ports are not trunked with one of the GE ports, then the FE ports operate as individual FE ports; see figure 20).

23. Kalkunte discloses the use of flow control (see col. 36 lines 50-55), *transmit modules* (MAC_TX_FIFO **140**; see figure 10) and *input modules* (input FIFO **142**; see figure 14). Kalkunte does not disclose memory that interacts with all the MAC interfaces. Moran discloses *receive* (receive store **30** allocated in memory **14**; see paragraph 0032) *and transmit modules* (transmit store **29** allocated in memory **14**; see paragraph 0032) *which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces* (figure 1 shows a bus is used to send and receive information between memory **14** and all the MAC interfaces **14**) *and storing the data packets in buffers associated with the plurality of MAC interfaces, each MAC interface being associated with a separate buffer* (see paragraph 0032). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Moran's arrangement in Ting's invention to control the amount of bandwidth for a port (Moran, title).

24. For **claim 25**, Kalkunte suggests *providing a control signal to determine whether the MAC interfaces operate as FE interfaces or whether the at least one interface operates as a GE interface* (when trunking is used, the members of a trunk group are assigned a trunk group index; see col. 36 lines 34-50).

25. **Claims 28-29** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ting in view of Moran.

26. For **claims 28 and 29**, Ting discloses *a plurality of Media Access Control (MAC) interfaces* (NIC **134**; see figure 1) *configured to receive/transmit Fast Ethernet (FE) packets* (see col. 4 lines 15-16)*; at least one MAC interface* (NIC **134**) *configured to receive/transmit Gigabit Ethernet (GE) packets in a first mode of operation* (Ting suggests this feature because NIC **134**

can have 10 Fast Ethernet device ports **136** that can be link aggregated via being assigned the same MAC address; see col. 1 lines 44-46 and col. 4 lines 12-16, 41-45) *and to receive/transmit FE packets in a second mode of operation* (if the device ports **136** are not link aggregated, the ports function as FE ports; see col. 4 lines 12-16)*; and wherein the ingress/egress port* (network interface **120**; see figure 1) *operates as a single GE port in the first mode of operation using the at least one MAC interface to transmit and receive GE packets* (since link aggregated device ports **136** share the same MAC address, the aggregated ports of the NIC **134** function as a single port; see col. 1 lines 44-46) *and as more a plurality of FE ports in the second mode of operation using the plurality and the at least one MAC interface to transmit and receive FE packets* (when the device ports **136** are not link aggregated, each device port **136** functions as a separate FE port; see col. 4 lines 12-16).

27. Ting discloses memory **108** and a storage interface **108** that are connected to *all the MAC interfaces* (NIC **134**) via network interface **120** and CPU **110** respectively (see figure 1). Ting does not disclose these memories as being transmit and receive memories. Moran discloses *receive* (receive store **30** allocated in memory **14**; see paragraph 0032) *and transmit modules* (transmit store **29** allocated in memory **14**; see paragraph 0032) *which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces* (figure 1 shows a bus is used to send and receive information between memory **14** and all the MAC interfaces **14**). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Moran's arrangement in Ting's invention to control the amount of bandwidth for a port (Moran, title).

28. Specifically for **claim 29**, Ting discloses *a switch* (trunk configuration routine **144**) *configured to switch the ingress/egress port between a first mode and a second mode of operation for the ingress/egress port* (the trunk configuration routine **144** switches the modes of the ports by assigning the same MAC address to ports that belong to a trunk; see col. 8 lines 50-55).

Response to Arguments

29. The arguments with respect to **claims 8-15, 16-17 and 19-25** are moot in view of the new grounds of rejection.

30. The arguments with respect to there being no motivation to combine Ting and Moran because Ting teaches increasing bandwidth while Moran teaches reducing bandwidth are not persuasive. Ting discloses only links having the same data rate can be aggregated (see col. 4 lines 40-45). Therefore, there exists a situation where too much bandwidth may be assigned to the link. For example, if only 850 Mbps is needed, but according to Ting only 900 Mb of bandwidth can be link aggregated because the FE ports operate at 100 Mbps. The person of ordinary skill would turn to Moran to prevent from overloading a system by providing too much bandwidth to the link (see paragraph 0004).

31. The arguments with respect to Ting not disclosing an ingress/egress port having a plurality of MAC interfaces are not persuasive. The **claim 28** defines an ingress/egress port as having a plurality of MAC interfaces. Ting's network interface is essentially the same as the claimed ingress/egress port because figure 1 shows the network interface has a plurality of MAC interfaces.

32. Applicant's arguments filed 07/14/2010 have been fully considered but they are not persuasive, for the reasons stated above.

Allowable Subject Matter

33. **Claim 31** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

34. The following is a statement of reasons for the indication of allowable subject matter: the combination of Kalkunte, Moran, Takeuchi and Gentry suggests the *extracting eight two byte items* (enough bytes of a packet need to be captured such that one or more protocol headers are captured; Gentry, col. 13 lines 25-37). According to the combination, the header information is stored in a *memory bank* (header memory **302**; Gentry, col. 13 lines 39-52). However, the combination does not disclose the particular placement of the header information in the header memory **302**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY M. RUTKOWSKI whose telephone number is (571)270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeffrey M Rutkowski/
Examiner, Art Unit 2473

/KWANG B. YAO/
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